53 Gbps Optical Link with Co-designed DSP and Integrated EAM Driver, Heterogeneously-Integrated Transmitter, and Monolithically-Integrated Receiver

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***Abstract*—We demonstrate an optical link at 53 Gbps using a 53G DSP with integrated electroabsorption modulator driver, a transmitter with heterogeneously integrated tunable lasers and electroabsorption modulators, and a receiver with monolithically integrated photodetectors and transimpedance amplifiers.**

Keywords—Silicon photonics, optical communication, heterogeneous integration, monolithic integration, electronic-photonic co-design

I. Introduction

Devices manufactured in silicon photonics thin-SOI foundry processes have historically underperformed their counterparts in other material systems such as indium phosphide, gallium arsenide, or lithium niobate in raw performance metrics such as modulator Vπ or responsivity. Silicon photonics device manufacturers surmounted these performance woes by taking advantage of the tremendous silicon wafer manufacturing ecosystem and tools to offer cost-competitive devices at "good-enough" performance [1]. However, in recent years, several foundries and foundry partners have developed novel integrations into the traditional silicon photonics flow that now enable simultaneous lowest-cost and highest-performance alongside the benefits of silicon economies of scale [2, 3].

In this manuscript, we utilize these new foundry offerings to construct an optical link operating at 53.125 Gbps PAM4 and 53.125 Gbps NRZ. Three types of integration are showcased in this measurement: (1) co-integration of optical device drivers with a TX & RX PHY in a DSP fabricated in an advanced CMOS foundry, (2) heterogeneous integration of III-V devices onto a silicon photonics platform, and (3) monolithic integration of 45nm CMOS transistors with silicon photonics passive and active devices.

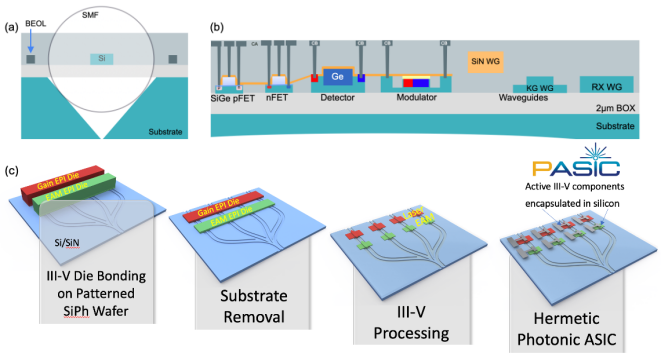
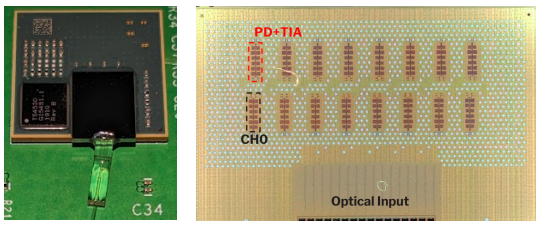


Fig. 2. Novel photonic integration platforms used in the transmit and receive chips: (a) Monolithic 45nm CMOS and photonics co-integrated on the same wafer and (b) Heterogeneous III-V devices bonded to a silicon photonics wafer.

II. Silicon Device Integration

The DSP chip is fabricated in an advanced FinFET process with the electroabsorption modulator driver monolithically integrated and co-designed with the TX PHY output. The transmit OpenLight SiPho 4-channel coarse wavelength division multiplexing (CWDM) Photonic Integrated Circuit (PIC) is fabricated in the Tower Semiconductor PH18DA process [4]. A conceptual drawing of the fabrication flow is shown in Fig. 1(b): The SOI wafer is patterned with photonic devices, then a III-V die is bonded to the top surface of the wafer and the III-V die substrate is removed. The III-V device area is further processed and patterned. Finally, the back end of line metal interconnects are formed. Through this process, a single silicon photonics wafer can support multiple types of III-V device functionality. In this example, a III-V gain region is used to form tunable lasers and a separate III-V electroabsorption regime is used to form the heterogeneous silicon/III-V electroabsorption modulators. The TX PIC was flip-chipped onto a metal-organic substrate. A low-loss edge coupling pigtailing process was used to couple light from the PIC to SMF fiber as shown in Fig. 2a.

The 16-channel receive chip is fabricated in the GlobalFoundries Fotonix™ process that monolithically integrates 45nm CMOS devices and photonics on the same SOI wafer [3]. A cross section illustration is shown in Fig. 1(a). The receive chip incorporates a high-speed transimpedance amplifier, including cascaded stages of a shunt-inverter TIA section, inverter-based Cherry-Hooper amplifier, variable gain amplifier, continuous time linear equalizers, pre-driver, and output pad-driver [5]. On-chip bias current generation and monitoring functionality is also



(a) (b)

Fig. 1. (a) Flip-chip assembled PIC with edge coupled fiber pigtail. (b) Die image of the receive chip with integrated spot size converter, polarization splitter & rotator, tap-photodetectors for monitoring, and high-speed PD+TIA circuit.

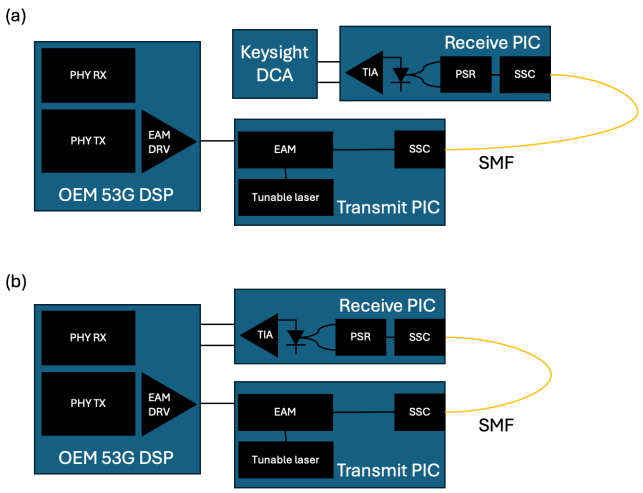


Fig. 4. Block diagram schematic of the optical link test setup. (a) A Keysight DCA is used to capture the output eyes from the TIA and (b) the DCA is removed for bit error rate loopback measuremenbts.

implemented and the entire chip utilizes a digital SPI controller to read & write on-chip registers. A V-groove spot-size converter brings light from standard 10µm MFD single-mode fiber to on-chip waveguides, while on-chip polarization splitters & rotators enables polarization diversity into the high-speed photodetectors.

III. Optical Link Experiment

The block diagram schematic of the experimental setup is shown in Fig. 3. The TX EVK was connected to the DSP EVK with 12 inch RF cables, with an additional total 4 inches of PCB transmission lines on the respective EVK boards. To measure eye diagrams, the receive PIC TIA output is connected to a Keysight digital communication analyzer (DCA) as in Fig. 3(a) with 14 inches of coaxial RF cables. For bit error rate testing, the TIA output is directed through 20 inches of coaxial cables to the 53G DSP. DC blocks are used between the TIA output and both the DCA and the 53G DSP chip since the TIA has a common mode voltage output of 0.9 V. The RF losses in the test setup are similar to a linear drive scenario [6], showing feasibility of LPO SiPho modules. SMF fiber is used to directly connect the transmit PIC modulated output to the receive PIC. The DSP chip contains a feed-forward equalizer (FFE) in the PHY TX, which is used to compensate for any bandwidth limitations in the transmit PIC. The DSP PHY RX utilizes an adaptive equalizer.

Measured eye diagrams at 53.125 Gbd NRZ and 26.5625 Gbd PAM4 are shown in Fig. 4. The NRZ eye in Fig. 4(a) and PAM4 eye in Fig. 4(b) is without any additional DSP processing on the DCA. The eye shown in Fig. 4(c) is with offline processing in the DCA to implement a 5-tap TDECQ feed-forward equalizer filter. The reported 1.91 dB TDECQ value of the TIA electrical eye is measured through the entire DSP to transmit PIC to receive PIC chain. Typically, TDECQ values are reported for transmitter eye quality, but one is used here to demonstrate overall link quality.

The DSP chip contains an integrated bit error rate monitor. At 26.5625 Gbd PAM4 and 150 µA average photodetector current measured through the photodetector bias pin, a stable 1e-6 BER is measured before any forward error correction. At a 170 µA average photocurrent, the 56.125 Gbd NRZ signal

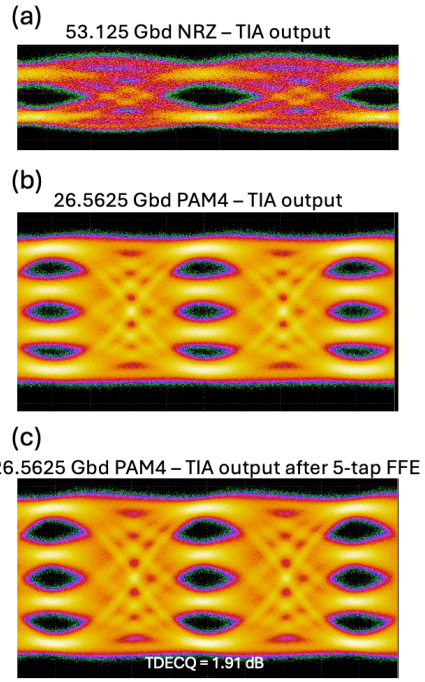


Fig. 3. Measured electrical eye diagrams from the DCA at (a) 53.125 Gbd NRZ, (b) 26.5625 Gbd PAM4, and (c) 26.5625 Gbd PAM4 after a 5-tap TDECQ FFE.

is received error-free (BER<1E-12) without any forward error correction.

IV. Conclusion

We have demonstrated an optical link at 53.125 Gbps PAM4 and 53.125 Gbps NRZ where the DSP chip incorporates a co-designed PHY and EAM driver, the transmit photonic chip heterogeneously integrates III-V devices to form tunable lasers and electroabsorption modulators, and the receive photonic chip monolithically integrates CMOS electronics and photonics. This demonstration of an optical link with leading-edge silicon photonics process nodes paves the way for future silicon photonic chips to leverage the same process integrations for next-generation systems.

Acknowledgment

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References

[1] M. Streshinsky, A. Novack, and S. Ardalan, "Enabling the Next Generation of Photonics through Design IP Reuse." In *2023 International Conference on Photonics in Switching and Computing (PSC)*, 2023

[2] Baets, Roel. "Heterogeneous integration in silicon photonics." In *IEEE Photonics Conference (IPC)*. 2022.

[3] M. Rakowski, et al., "45nm CMOS - Silicon Photonics Monolithic Technology (45CLO) for next-generation, low power and high speed optical interconnects," in *Optical Fiber Communication Conference* (OFC), paper T3H.3, 2020.

[4] https://openlightphotonics.com/technology

[5] T. Baehr-Jones, et al., "Monolithically integrated 112 Gbps PAM4 optical transmitter and receiver in a 45 nm CMOS-silicon photonics process," Optics Express, vol. 31, no. 15, pp. 24926-24938, 2023

[6] "Linear drive enables green all-optical connectivity for datacenters–webinar," https://www.lightcounting.com/resources#